

# Petaflops Device Technologies

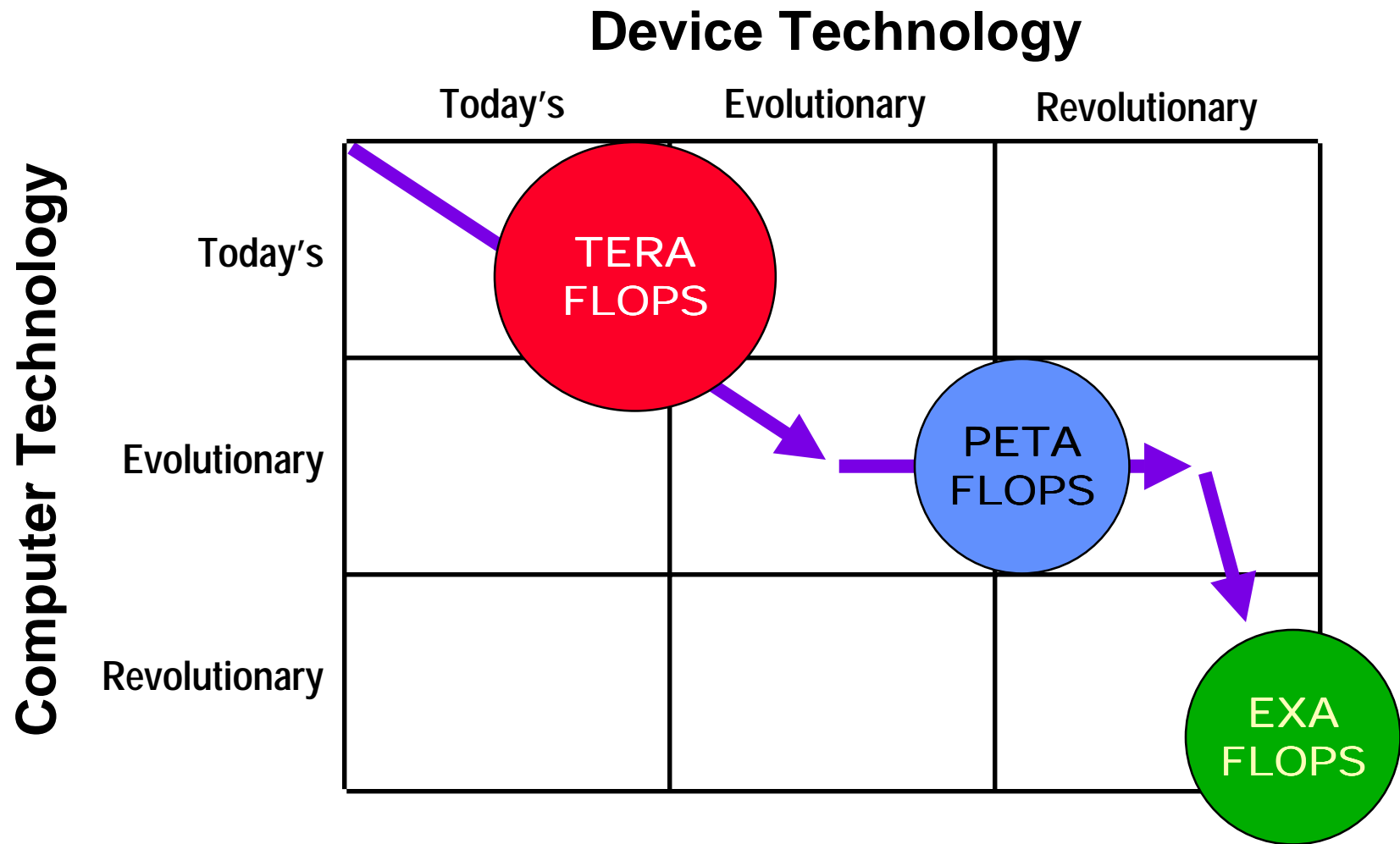
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# Outline

- ◆ Review Petaflops-1 projections of enabling device technologies for petaflops computing systems
- ◆ New device technologies for petaflops computing

# Revolutionary Leapfrogs Evolutionary



# Reflections on Petaflops-1

## Keynote Addresses

# Reflections on Cray Keynote Address

- ◆ The *lunatic fringe*
- ◆ \$80 K/Gflop cost in Cray 4 (excl. memory)
- ◆ 4 X improvement projected every 4 years
- ◆ \$50 M for *Teraflops* machine (incl. memory)
- ◆ Maybe another factor of 1000 to *petaflops* in another 20 years
- ◆ Revolutionary approaches will be necessary to achieve petaflops in 10 years
  - Reduce device size to nano scale
  - Look to molecular biology community
  - Use biological devices to manufacture non-biological devices

# Reflections on Likharev Keynote Address

- ◆ Revolution in digital superconductor electronics – RSFQ circuits
- ◆ Josephson junctions
  - Picosecond data pulse generation
  - Millivolt signals implies low dissipation
  - Impedance matched to transmission lines
- ◆ Superconducting transmission lines
  - “Ballistic” transfer of picosecond pulses at speed of light
  - Small crosstalk
- ◆ High gate density at high speed
- ◆ Simple fabrication technology

## Reflections on Likharev Keynote Address-2

- ◆ Intrinsic quantization at very small levels
- ◆ Clock rates at 100 GHz with 3  $\mu\text{m}$  design rules
  - Projected to 300 GHz at 0.35  $\mu\text{m}$  design rules
- ◆ Projected 100 Gflops per processor at 1  $\mu\text{m}$  design rules
  - 100 GHz clock
  - 100 mW per processor at 4 kelvin
  - $10^5$  processors for PF
  - 1 kW power dissipated in LHe
  - 300 kW total power
  - Plus memory
- ◆ Large memory needed
- ◆ \$\$ needed to make it happen

# Report of Petaflops 1

## *Enabling Technologies for Petaflops Computing*

Thomas Sterling, Paul Messina, and Paul H. Smith

MIT Press 1995

- ◆ First workshop held in January 1994 in Pasadena, CA
- ◆ Sponsored by six federal agencies:  
NASA, NSF, DOE, ARPA, NSA, BMDO
- ◆ Goal was to produce the first comprehensive assessment of technologies needed for petaflops computing systems
- ◆ Four Working Groups
  - Applications and Algorithms
  - Device Technology
  - Architecture
  - Software Technology

# Barriers Beyond Teraflops

## Identified by Architecture Group

- ◆ Clock speed of silicon microprocessors
- ◆ Cost is a dominant obstacle
  - Brute force methods would cost [\$B 100's]
  - Dominated by memory
- ◆ Diameter measured in clock cycles would be extremely broad
- ◆ Requires levels of memory bandwidth, latency hiding, and fine-grain parallelism orders-of magnitude beyond experience
- ◆ Reliability and programming methodologies

# Petaflops-1

## Device Technology Working Group

Carl Kukkonen, JPL	Chair
John Neff, Univ of Colorado	Co-Chair
Doc Bedard, NSA	Co-Chair
Joe Brewer, Westinghouse	Co-Chair

### Questions Addressed

- ✓ State-of-the-art?
- ✓ Level of investments?
- ✓ Focus of advanced work?
- ✓ Estimated rate of progress in terms of key FoM?
- ✓ Barriers and challenges?
- ✓ Potential opportunities for significant evolutionary & revolutionary advances?
- ✓ Accomplishments and likely rate of progress in terms of FoM?
- ✓ Order-of-magnitude investment required to achieve goals?

# Three Device Technologies Considered Most Likely to Provide Basis for Implementation of Petaflops Computing

- ◆ Advanced semiconductors
  - ❑ Main memory
  - ❑ Possibly processor logic
- ◆ Optical devices
  - ❑ High bandwidth intermodule interconnect
  - ❑ Mass storage
- ◆ Superconducting elements
  - ❑ Very high speed processors at very low power dissipation
  - ❑ Very high clock frequencies

# Advanced Semiconductors Was Memory Candidate

- ◆ CMOS VLSI
  - ◆ SIA Moore's Law projection out to 2007
    - 0.1  $\mu\text{m}$  features
    - 20 M logic gates per chip
    - 16 B bits DRAM
  - ◆ Power will be an issue for petaflops processor
  - ◆ Projections of GaAs impact premature
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- ➔ Application in HTMT Baseline Design
    - SRAM-PIM
    - DRAM

# Optical Devices Were Candidates for WB Comm and Memory

- ◆ Opportunity to significantly increase performance at lower power than semiconductors
  - ◆ Medium to long-range communications,
    - Guided fiber and free space
    - Particularly as BW increases by orders-of-magnitude
  - ◆ High density secondary storage
    - 2-photon and spectral hole burning 3-D technologies
  - ◆ Most likely incorporated in a hybrid architecture
  - ◆ *Does not* appear suited to logic applications
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- ➔ Application in HTMT Baseline Design
    - Fiber-optic Data Vortex network
    - 3-D HRAM

# Superconductors Was Processor Candidate

- ◆ Combination of
    - ❑ Clock speeds 10 to 100 X faster than semiconductors
    - ❑ Projected to 50 GHz by now
    - ❑ 10 to 100 X power-delay advantage
  - ◆ 4 kelvin environment viewed as negative
    - ❑ Need for cooling to 4 K
    - ❑ Interfacing to 4 K at required BW
  - ◆ Lack of funding due to absence of strong market pull
  - ◆ Clearly a candidate for 1000 processor petaflops system
    - ❑ Limited superconductor memory capability expected
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## ➔ Application in HTMT Baseline

4096 processors

CRAM

CNET

# Petaflops-1 Was a Prescient Predictor of Enabling Device Technologies for HTMT Baseline Design

- ✍ RSFQ cryogenic processors
- ✍ Limited superconductor memory (CRAM)
- ✍ SRAM/PIM
- ✍ Fiber-optic data vortex network
- ✍ DRAM
- ✍ HRAM
- ✍ Wideband cryogenic I/O is difficult
- ✍ Progress in superconductor processor technology was limited by funding during 1990's

# Emerging Technologies Circa 2000?

- ◆ Resonant tunneling devices (RTD)
- ◆ Metal-semiconductor transitions
- ◆ Opto-electronics
- ◆ Nano-technology
- ◆ Single electron transistors (SET)
- ◆ Quantum dots
- ◆ Biological systems

# What About Quantum Computation?

- ◆ Is there a practical device technology?
- ◆ Can we contemplate scaling to petaflops?