

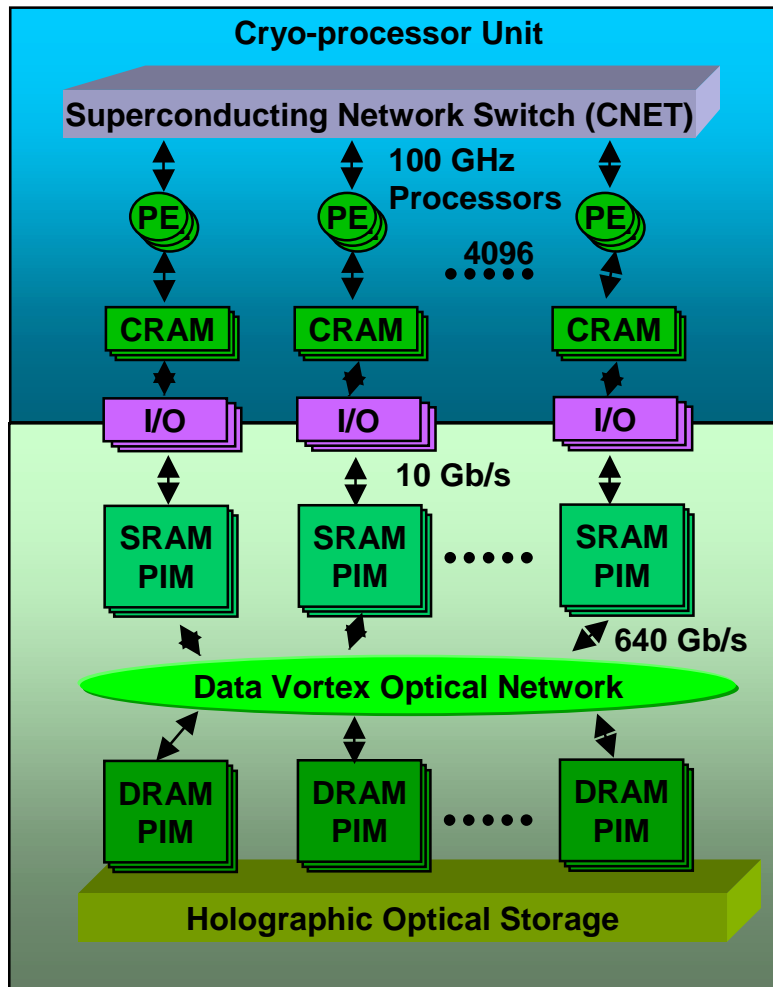
Full-Scale Integration of Superconductor Electronics For Petaflops Computing

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Q. Herr, G. Kerber, M. Leung, and T. Tighe**

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Technologies for Petaflops Computing
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Hybrid Technology Multi-Threaded Computer



- **Hybrid Technology**

- 100 GHz SCE Processors (RSFQ)

- Processor in Memory (PIM) SRAM/DRAM

- Terabit optical network (WDM)

- Holographic memory (Spectral hole burning)

- **Multi-Thread**

- multi-stage latency management

- memory “percolation”

- Coarse grain multithreading

- PIM smart memory management

Impact	TODAY	HTMT	IMPROVE
PERFORMANCE	1 Teraflops	1000 Teraflops	X 1000
POWER	2 Mflops/W	1000 Mflops/W	X 500
COST	\$250/Mflops	\$0.25/Mflops	X 1000
EFFICIENCY	10%	50%	X 5
FLOORSPACE	1600 sq ft/Tflop	1 sq ft/Tflop	X 1600

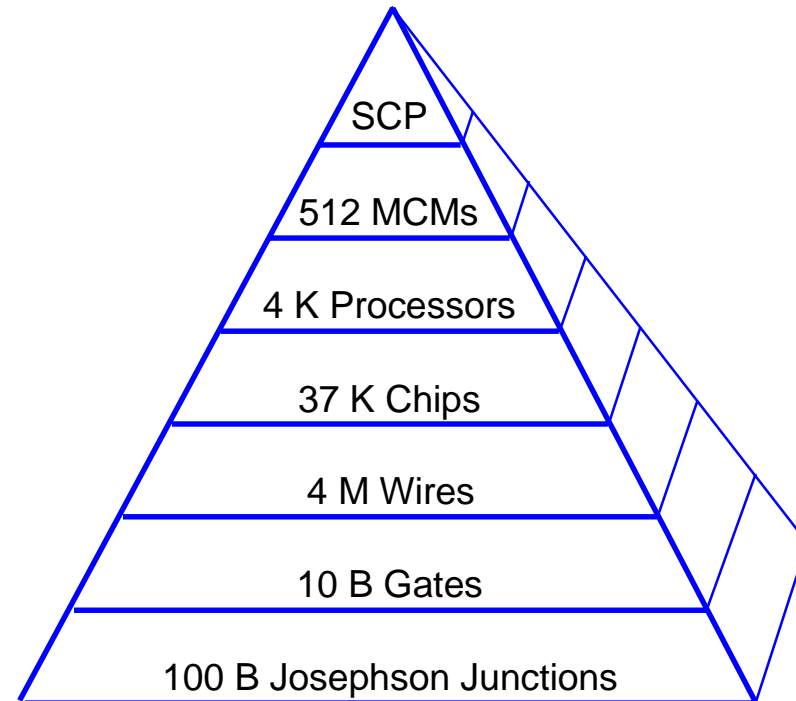
System Requirements Will Challenge ScE Technology

Feasibility/Manufacturability of ScE Processor in terms of:

- Integrability
- IC Manufacturing
- Packaging
- Data Interconnect
- Power Interconnect

Requirements:

- 100 GHz clock
- $J_0 = 20 \text{ kA/cm}^2$
- 300K gates/chip
- 2-5k pinouts/chip
- 50 chips/MCM
- 30 Gbps MCM-MCM BW
- 4M wires @ 8-10 Gbps



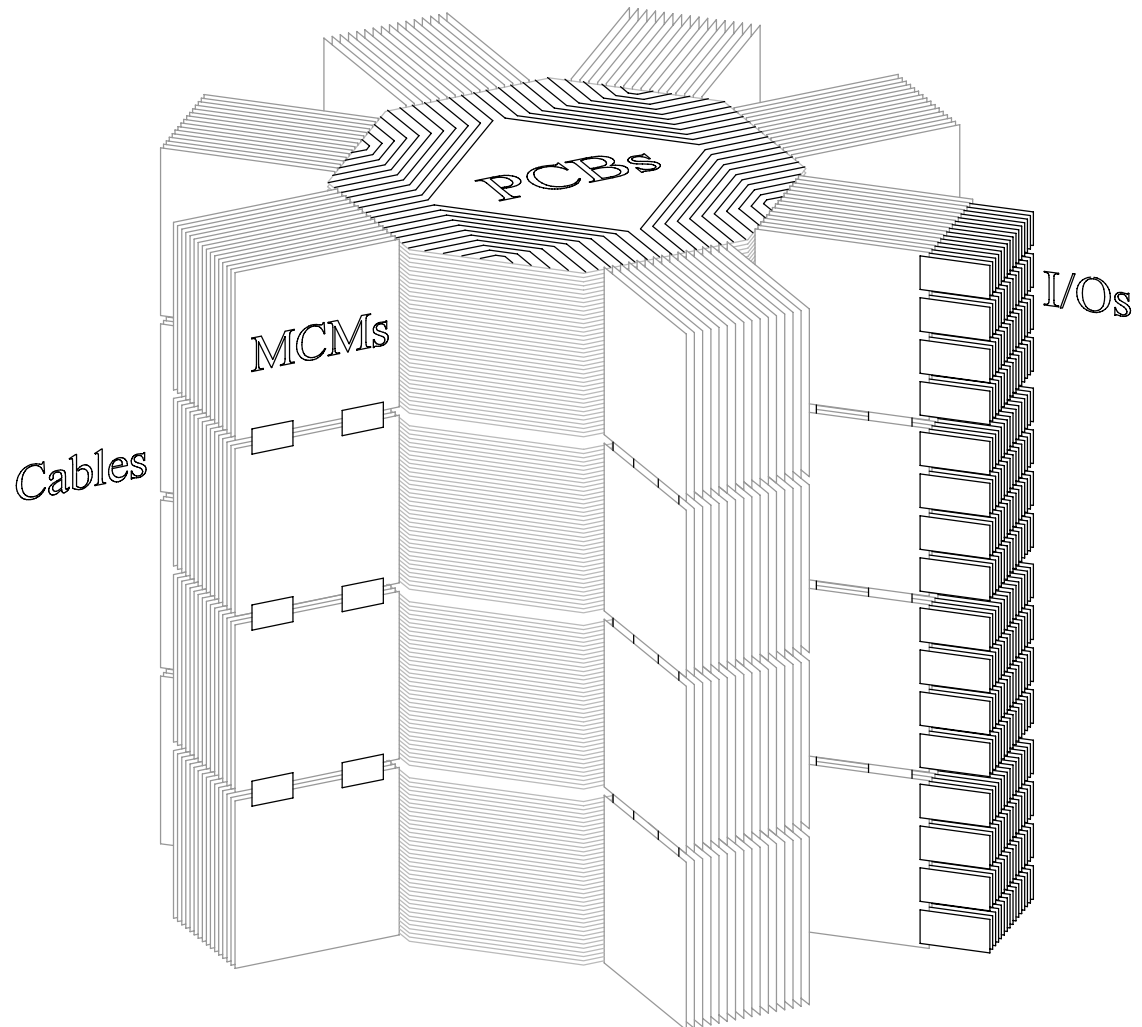
Low-Power Electronics Enables Compact Package



Issues:

- Chip Production (yield, defect density, known good die)
- Integrated Packaging (thermal, mechanical, electrical)
- Power Budget (on-chip/system power, power distribution)
- Interface/Interconnect Requirements (clocking, communications)
- Local Memory Implementation
- Physics, Cost, Schedule, Practicality

- 512 MCMs, 160 PCBs
- 1 m³ package, 1 kW @ 4 K



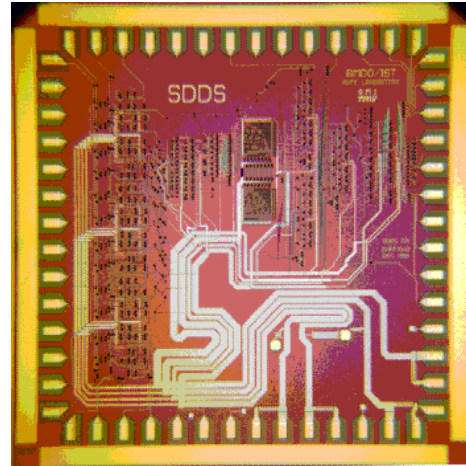
Producibility Issues Are Being Addressed



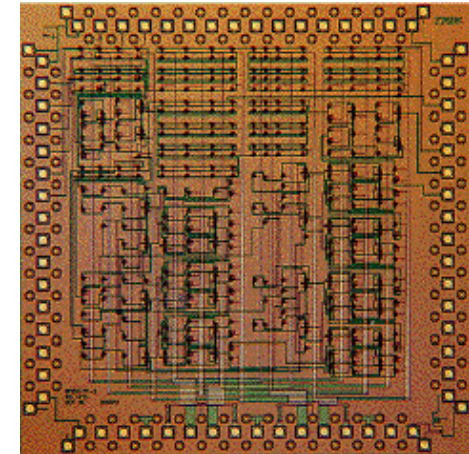
Component Topic	Stressing Requirements	Feasibility	Approach
Processor chips	Clock, Gate density	Probably	Advanced lithography More vertical integration
Memory chips	Density	Maybe	Advanced lithography More vertical integration
Chip attach	Pin density, inductance MCM Vendor fab	Yes	Solder reflow
MCM - MCM attach	Density, B/W	Probably	In evaluation
Data I/O	B/W No. of lines	In - Yes Out - Maybe	Optical fiber, WDM Ribbon cable, asymmetry
System assembly, Repairability	Modularity, B/W, repairability Disassembly, Repair	Maybe Maybe	3-D structure, Socketed Pin in sockets
Cooling	Power density Flow rates	Probably	LHe conduction cooling

Superconductor Electronics

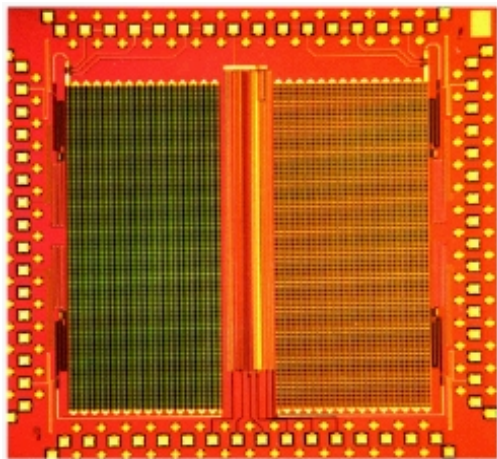
- Wideband analog electronics
- High clock rate digital electronics
- Ultra-low power
- Monolithic ICs
- Low noise, high sensitivity



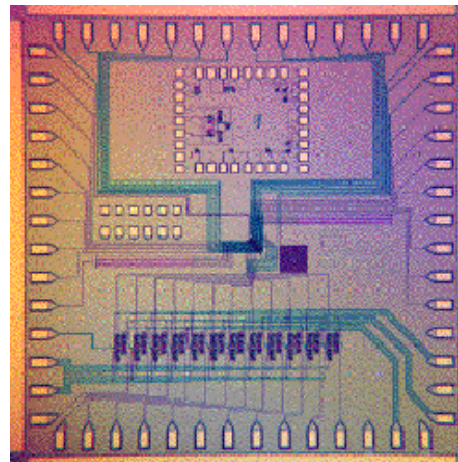
Digital frequency synthesizers



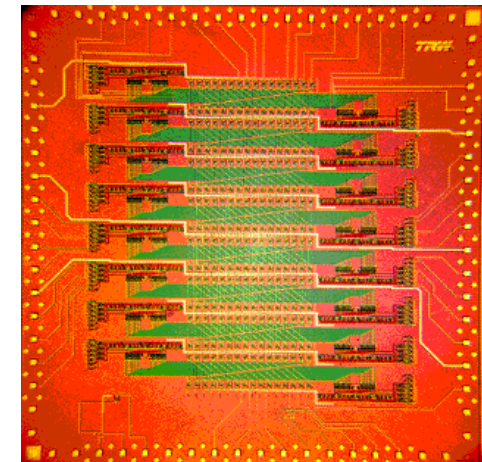
Low power, high speed digital signal processor



Wideband LNA
ELF/VLF/RF/VHF/UHF

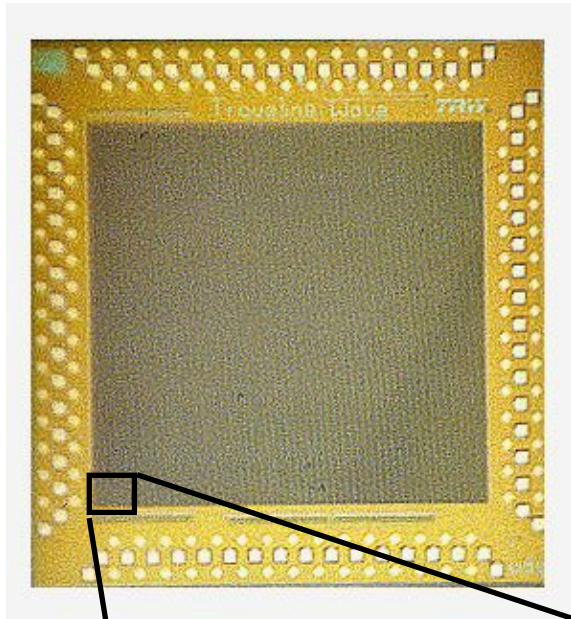


High res, wideband
A/D Converter

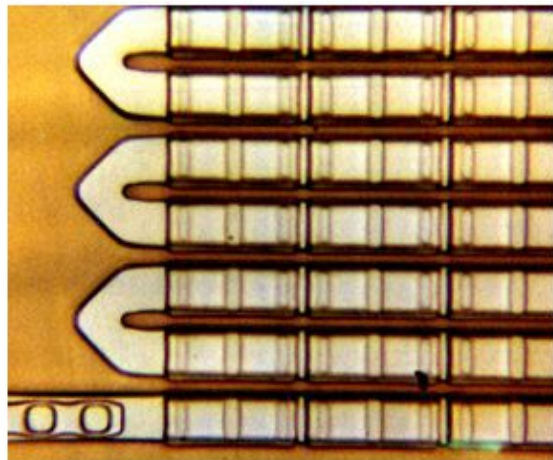


High data rate packet switch

Transmission Line Fabrication Uses Standard Foundry Design Rules



- 5mm square chip
- Up to 90,000 junctions per line
- Up to 1.2 meters of microstrip
- Standard TRW Nb process ("JJ110")
 - 2.5 micron min. junction dimension
 - 12 mask layers
 - Defect-tolerant design



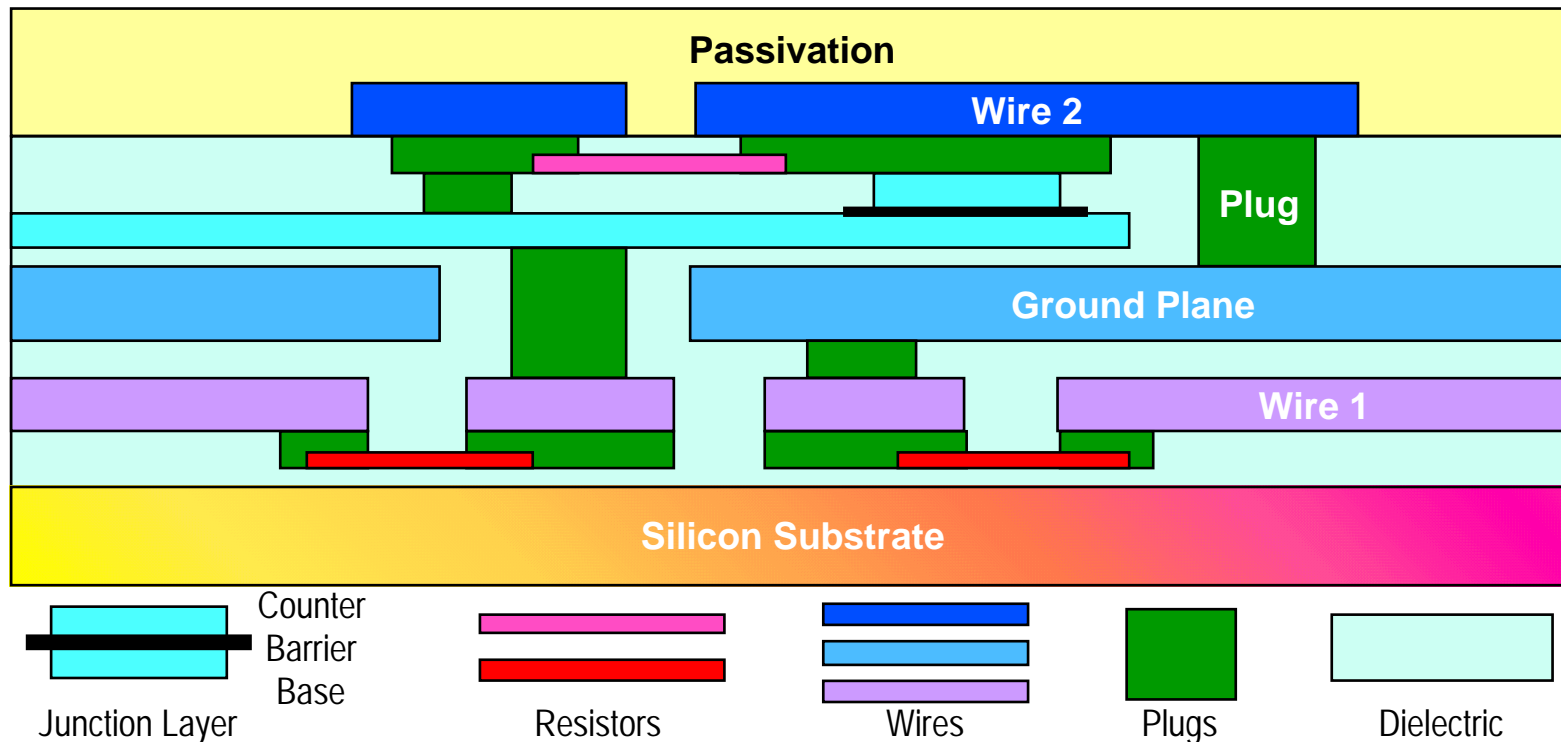
Advanced IC Process Can Reduce Latency



	Increased Clock Rate	Increased Density
Process Improvement	Smaller junctions with higher critical current density.	Smaller line pitch. Increased vertical integration.
Benefits	Higher junction impedance. Higher voltage signals.	Reduced latency.
Disadvantages	Larger electrical spreads. Increased latency.	Lower yield.

Latency is measured as the number of clock ticks for signal propagation from gate A to gate B.

Process Complexity Will Require Advanced Tools



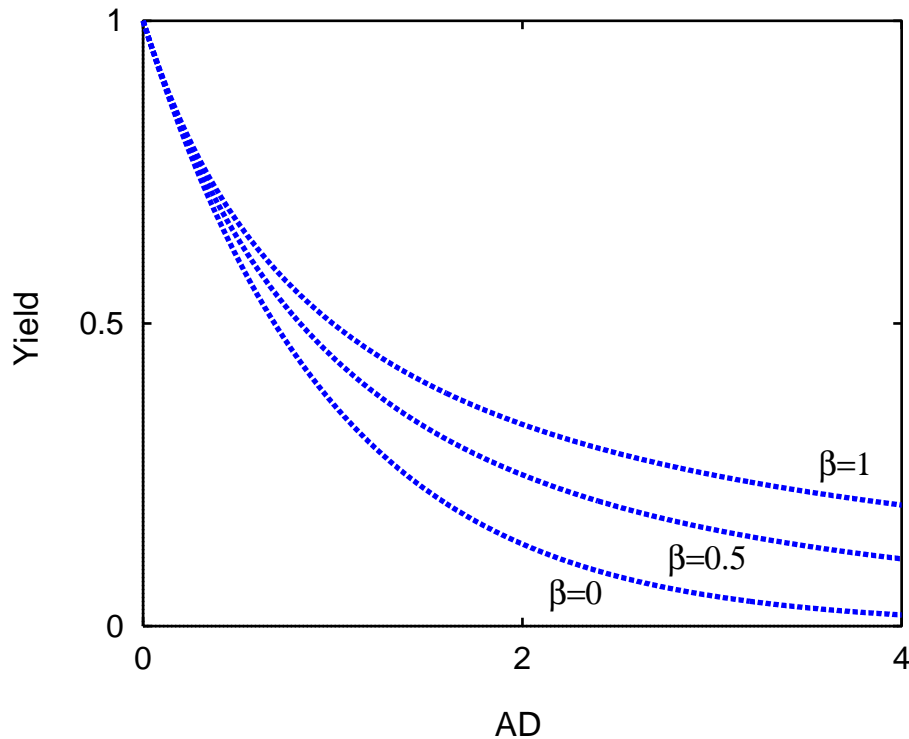
- Planarization
- Sub-micron lithography
- PLUG technology
- Resistor Development
- > 3M active devices/cm² at 0.8 μm design rule

Fabrication Yield Factors in Cost and Feasibility



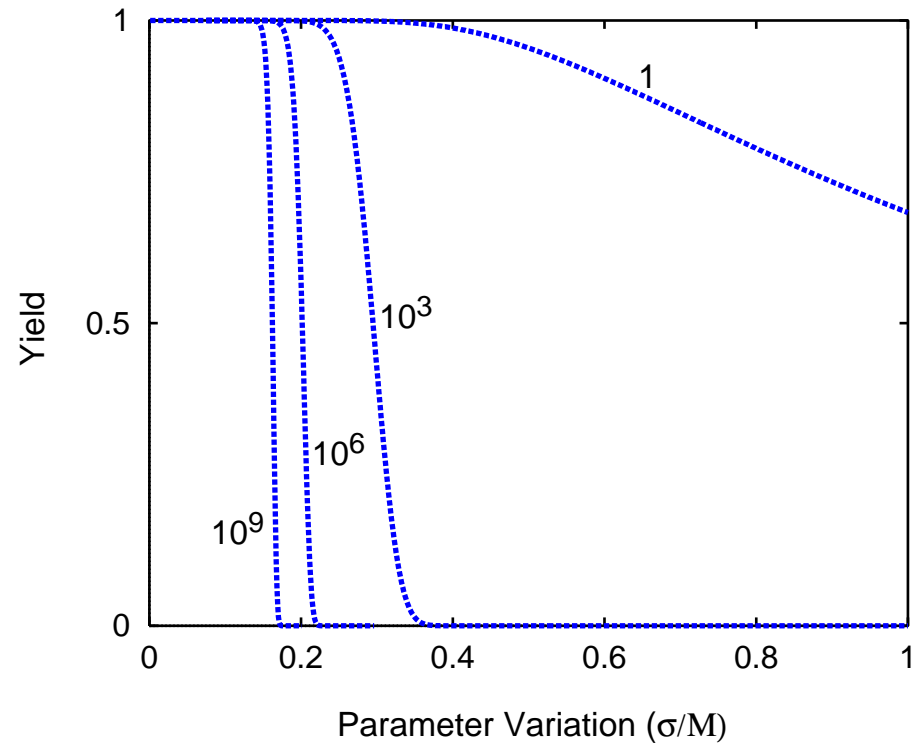
- ScE circuit yields unknown
- Trade-off complexity against spreads
- Chip size selection is critical design parameter

Yield Due to Defect Density



A.V. Ferris-Prabhu
Introduction to Semiconductor Device Yield Modeling

Yield Due to Parameter Spreads



Miller, Przybysz, and Kang, ASC '92

IC Technology Roadmap Scales Beyond PFLOPS



- Time scale is a function of resources
- 2004 IC technology is comparable to SIA 1992

	Year	1998	1999	2001	2004	2007	SIA*1992
Minimum Feature size (μm)		1.5	1.25	0.80	0.50	0.25	0.50
Junction size (μm)		2.5	1.75	0.80	0.80	0.80	-
Junction current density (A/cm^2)		2K	4K	20K	20K	20K	-
Gates/chip		5K	25K	120K	400K	1200K	300K
Chip size (mm^2)		100	200	400	400	400	250
Wafer diameter (mm)		100	100	150	150	150	200
Defect density (defects $/\text{cm}^2$)		< 2	< 0.5	< 0.2	< 0.1	< 0.05	< 0.1
No. of interconnects levels		3	4	4-5	5-6	6	3
No. of resistor layers		2	2	2	2	2	-
Planarization		no	yes	yes	yes	yes	yes
Self-aligned junction contacts		no	no	yes	yes	yes	-
No. of I/Os		128	750	2K	2-5K	2-5K	500
Wafer starts per month		12	16	200	1K	1K	>20K

* *The National Technology Roadmap for Semiconductors*, Semiconductor Industry Association, 1997.

Packaging Roadmap



	1998	2001	2004
MCM (Ceramic/Dielectric technology assumed)			
Pad size (μm)	100	75	25
Pad pitch (μm)	150	125	60
Number of pads per chip	3600	5000	12000
Pad density (cm^{-2})	1200	2000	7500
Max. no. Nb layers	5	7	9
Max. no. W layers	20	40	100
Linewidth (μm)	5	3	3
Bandwidth (Gbps/wire)	10	10	30
Chip-to-chip SFQ?	No	Yes	Yes
Chips per MCM	24	75	100
Backplane			
Technology	PCB	Ceramic	Ceramic/Flex
Size (cm^2)	30	30	50
Bandwidth (Gbps/wire)	2.5	5	10
I/O ribbon cables			
Line pitch (μm)	200	50	10
Cable width (cm)	2.5	5	5
Bandwidth (Gbps)	2.5	5	8
Heat load/wire (mW @ 4K)	0.4	0.2	0.1

Chip Attach Strategy: Flip-Chip Bonding

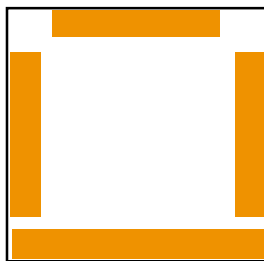


Requirements:

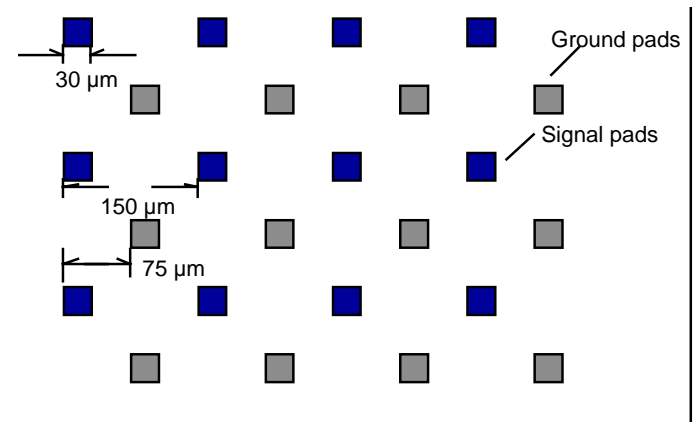
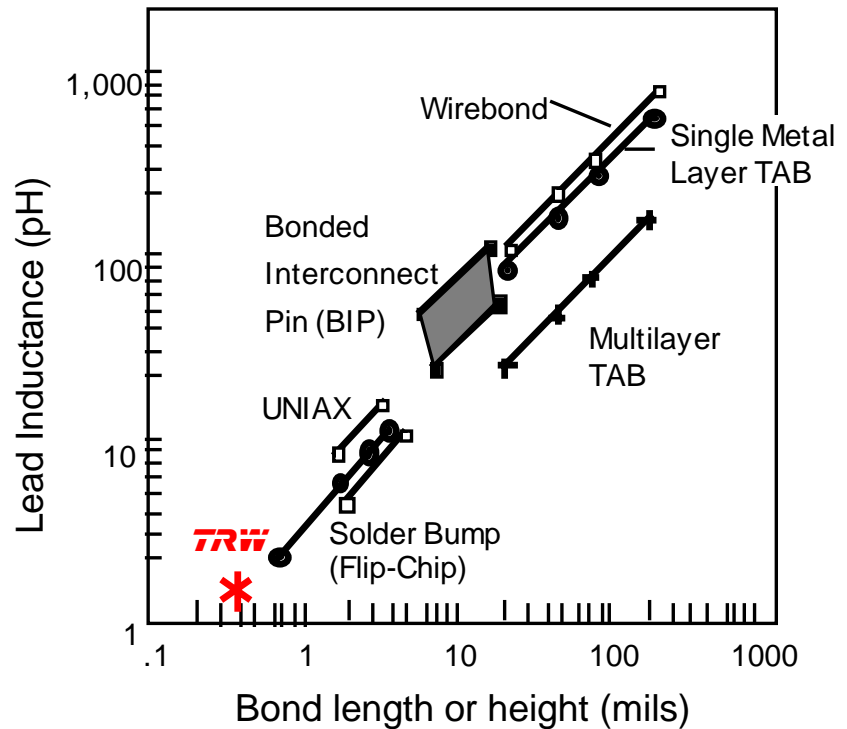
- low inductance interconnects
- 12,000 pads/chip

TRW has demonstrated bumps:

- ~1 pH (6-7 μm high)
- 25 μm diameter, 60 μm pitch



25% of 2 cm PNET/PMI/FPU

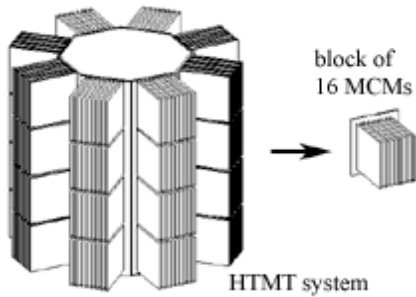


30 μm bumps, 150 μm pitch

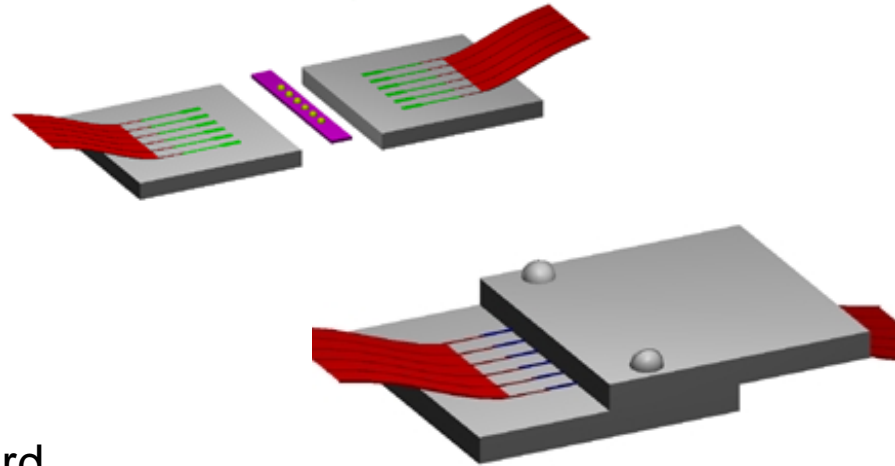
Building the System



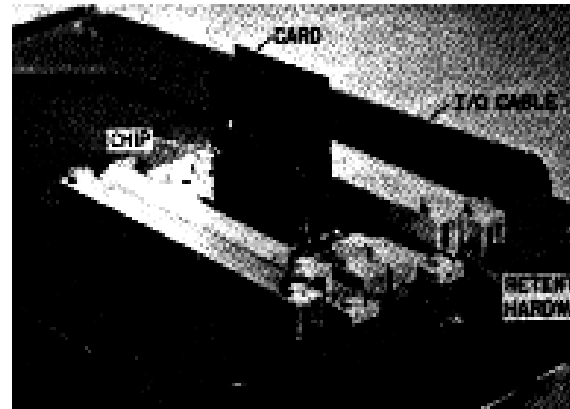
- Modularity



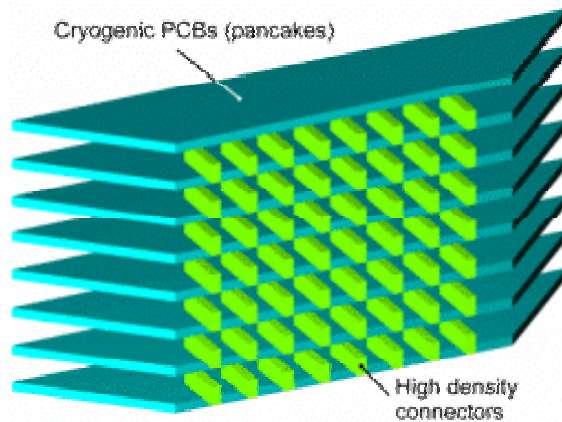
- Detachable flex cables/fiber optic cables



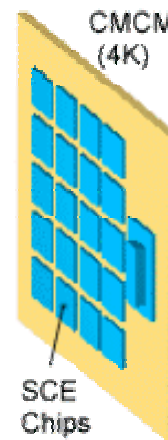
- Motherboard/daughterboard



Module Strategy: Plug and Play



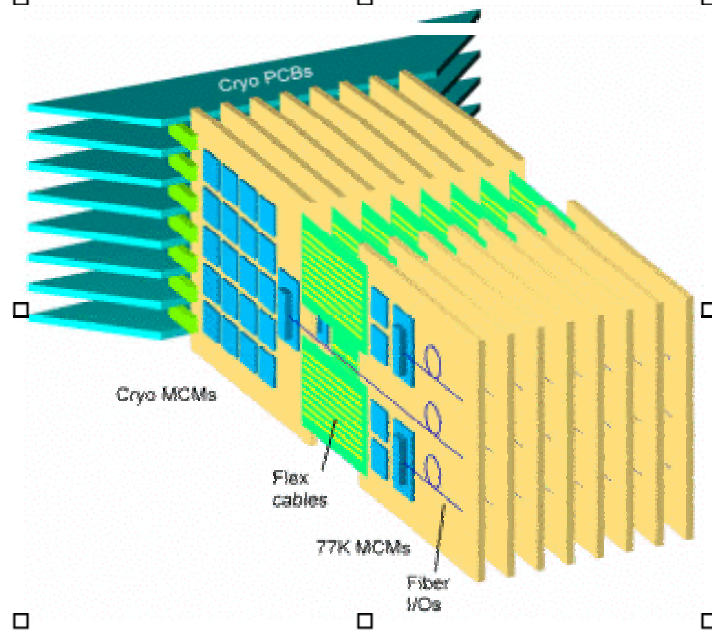
Pancakes



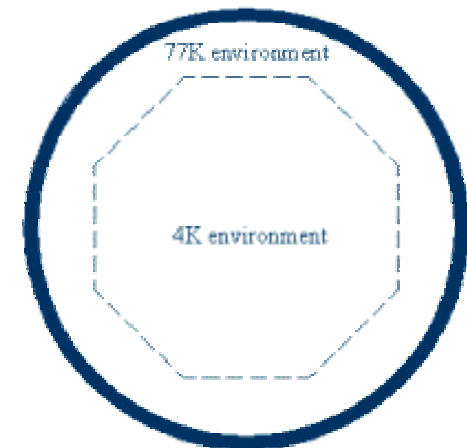
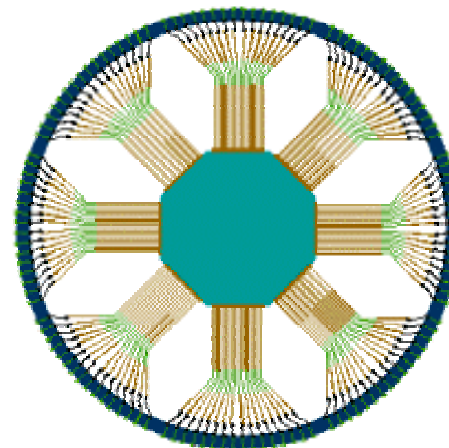
4K CCMs



77K MCMs



Assembled block of MCMs



Top view of assembled system

Cooling Requirements at 4 Kelvin



Heat Load at 4 K

	Worst Case	Best Case
Circuit Dynamic Power	250 W	250 W
Circuit Static Power	1250 W	0
Total for Cu I/O	600 W (8 M lines @ 70 μ W/line)	10 W (125 K lines @ 70 μ W/line)
TOTAL	2100 W	260 W

Example: 2 kW Refrigerator at Karlsruhe

	Refrigerator	Liquefier
Refrigeration at 4 K	1500 W	
Capacity		650 liters/hr
Wall Power	620 kW	780 kW
Efficiency	413 W/W	

Physical size is 25 m x 17 m x 10 m, including compressors, cold box, LHe tanks, and control.

Power

- Reduced power requirements enables use of HTS cables
- Overall system cooling not an issue
- Cooling by conduction eliminates cryogenic vacuum feedthroughs

Design/Test

- Address issue of latency and impact on integration level
- Total chip power (eliminate bias resistors)
- BIST, fault tolerant design
- CRAM implementation

Packaging

- Overall system concept
- CNET/SCP connection not resolved

I/O

- Chip-to-chip at 30 Gbps
- Electro-optical approach is favorable (fiber in, wire out)
- SRAM at 80K will impact power budget

ScE Is Enabling Technology For PFLOPS



- Technology goals are aggressive, yet achievable
- Fabrication tools exist, circuit yields unknown
- 1 m³ package reduces latency
- 1 kW heat load at 4 K is feasible